Spin Electronics, Spin Transfer Torque Magnetic Random Access Memory, Perpendicular Magnetic Anisotropy, Write Error Rates _____

Voltage and size dependence on write-error-rates in STT MRAM down to 11 nm junction size

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Abstract—The dependence of the write-error-rate (WER) on the applied write voltage, write pulse width, and device size was examined in individual devices of a Spin Transfer Torque MRAM 4 kbit chip. We present 10 ns switching data at the 10^{-6} error level for 655 devices, ranging in diameter from 50 nm to 11 nm, to make a statistically significant demonstration that a specific magnetic tunnel junction stack with perpendicular magnetic anisotropy is capable of delivering good write performance in junction diameters range from 50nm – 11 nm. Furthermore, write-error-rate data on one 11 nm device down to an error rate of $7*10^{-10}$ was demonstrated at 10 ns with a write current of 7.5 uA, corresponding to record low switching energy below 100 fJ.

I.   INTRODUCTION

Spin transfer torque switching [Slonczewski 1996] and magnetic tunnel junctions [Moodera 1995, Parkin 2004] opened a way for developing magnetic random access memory (MRAM). But only recently, after the discovery of perpendicular magnetic anisotropy (PMA) [Worledge 2011, Ohno 2010] in ultra-thin CoFeB layers, has MRAM become a promising nonvolatile memory which can be compatible with photolithographic line widths below 20 nm. Material investigations often concentrate on the quasistatic magnetic properties of novel materials at the level of unpatterned films [Karr 2013]. However, even the switching voltage, at 50% switching probability and at short ~10 ns write times, is not a good predictor of MRAM performance because of the possible presence of rare dynamic switching errors [Min 2010]. Accurate evaluation of novel materials for high density STT MRAM requires detailed examination of STT switching data in the nanosecond range and at write-error rate (WER) levels below 10^{-6}.

Patterning of ultra-small MTJs with novel materials and stack designs is challenging due to strong interaction effects between the new materials and the device fabrication process. As a result, in the early stages of the development of new materials, the yields of ultra-small devices are low and standard memory tests are difficult. To address these issues, we developed special digital tests which are capable of identifying and analyzing the well-performing individual MTJ's [Robertazzi 2013]. In this letter we demonstrate that a single MTJ stack with PMA materials is capable of delivering good

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STT performance down to 11 nm device size. We show statistically relevant STT switching data at WER = 10^{-6} for 655 devices with diameters ranging from 50 nm to 11 nm. We further show detailed WER curves for three individual devices with 40, 25, and 11 nm diameters, and demonstrate switching the 11 nm device at 10 ns with WER = $7*10^{-10}$ with only 7.5 uA.

II.   TEST DETAILS

The dependence of the write-error-rate on the applied write voltage, write pulse width, and device size was examined in individual devices of 38 STT MRAM 4kbit chips. Each of the 38 arrays had a different junction diameter. All tests were performed on a Verigy 93k logic/memory tester.

Each chip had separate write drivers for the "0" and "1" states and a sense amplifier circuit for fast read-out. The write and read times were controlled externally by the tester. All functional tests were performed with a relaxed cycle time of 250 ns to ensure reliable reading. A basic quasistatic parametric test was performed on the whole 4k array to identify reference voltages, the MTJ parallel-state resistance (Rp), and the tunnel magnetoresistance (TMR) for each individual device in the 4k array. A subset of devices from each array that had the highest TMR signal were selected for the WER test. The amplifier was set to an optimal reference voltage with the best readout margin. We did not preselect devices by their switching field (Hc) or other values.   The switching voltages for four long pulses (10μs, 100μs, 1ms and 10ms) were used to calculate the activation energy (Eb) [Min 2010]. Finally, a WER test was performed on individual devices by repeatedly exercising a read/reset/read/write sequence, typically over 1 million times, to reach a detection level of 10^{-6} errors per write at each voltage step. For a given

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write pulse duration, the dependence of the switching probability on write voltage was measured in the 0-700mV range. In all of the experiments, the junctions were reset using ±0.7 V at the same pulse width as the test pulse. The analysis of the WER data was done by real-time tallying of bit states in between each read/reset/read/write/read operation. The three read operation in this analysis sequence allowed identifying all of the possible error events: write and reset errors, state reversions related to read disturbs, and bit retention errors.
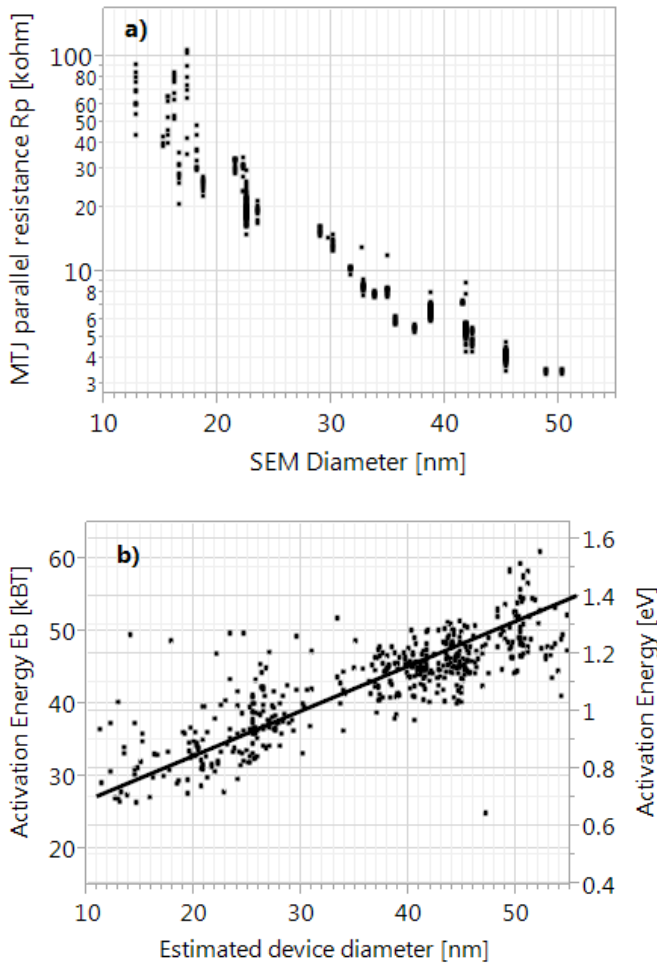

Figure 1 a) Rp dependence on SEM diameter and b) activation energy dependence on estimated device diameter for about 655 devices selected for WER measurements.

In total, 655 devices belonging to 38 different 4k arrays were tested for write-error-rate. All of the devices used the same MTJ stack, with an MgO tunnel barrier and a CoFeB-based free layer above the barrier; this was capped with another MgO oxide layer to enhance the perpendicular magnetic anisotropy (PMA) and reduce the spin-current loss related to spin-pumping [Tserkovnyak 2002, Konoto 2013].

The junction diameter for each 4k array was measured during fabrication by examining four randomly-selected devices using Scanning Electron Microscopy (SEM). Fig.1a

shows the correlation between the median of these SEM measurements and the Rp of the devices selected for these WER tests. The largest devices, about 51 ± 2 nm wide, had Rp ~ 3.5 kOhm, giving a resistance x area product (RA) of 7 Ohm-um^2. The smallest devices, measured by SEM, were ~12.5 nm ± 2 nm with Rp ~ 90 kOhm, giving an RA ~ 11 Ohm-um^2.The change of RA with device size likely resulted from an interaction between the MTJ materials stack and the fabrication process (damage of device edges). This median Rp versus SEM-size data was used to calculate an empirical function of RA versus junction size. This function was then interpolated to estimate the size of any individual junction in a 4k array.

Large devices (~50 nm) had Eb ~ 50 k_BT. For smaller devices, Eb decreased and approached ~30 kT at 10 nm device sizes. The bit stability below ~30 nm was not sufficient for 10-year retention, so for the smaller devices, materials with stronger PMA will be required.

III. WER RESULTS

Figure 2 shows the dependence of write error rate on write voltage and write time for 3 selected devices of different sizes. For each device, WER(V) curves are shown for write pulse widths of 10, 20, 50, and 100 ns.

For the 40 nm and 25 nm devices, we reached the requested 10^{-6} error floor with 10 ns write pulses at ~0.5 V and 0.67 V, respectively. Writing without errors was continued up to Vmax = 0.7 V (these data points cannot be seen on the logarithmic Y scale).

For most tests, the error floor was set at 10^{-6} due to test-time constraints. For the 11 nm device shown in Fig. 2c, however, the test time was increased for a deeper error floor detection of $7*10^{-10}$ with a corresponding increase of Vmax to 0.8 V. (The irregularities at deep WER levels in Fig. 2c originate from single errors per many million writes. In order to obtain smoother data at such deep WER levels, much longer test time would be required in order to average over more write cycles).

Shorter write pulses decreased the likelihood of encountering a thermal fluctuation large enough to initiate switching [Sun 2004]. For example, as shown in figure 2b for the 25 nm devices, the WER slope decreased from 111 decades/volt at 100 ns to 38 decades/volt at 10 ns. For smaller devices, the 10 ns write voltage threshold (at WER = 0.5) increased, but the WER slopes stayed similar ~ about 33 decades/volt (averaged over the two polarities). The change in the voltage required to reach the 10^{-6} level can be used to extrapolate the required voltages for future MRAM chips.

For the smallest devices shown in Fig. 2c, the voltages needed to reach the 10^{-6} error floor with 10 ns pulse widths were similar for writing "1" and writing "0" , but the slope in the 10^{-3} -10^{-9} range for writing "1" (V > 0) was about 27 decades/volt compared to 42 decades/volt for writing a "0", or about 35% smaller. This illustrates the important experimental result that, for ultra-small devices, it is much more difficult to write "1". Interestingly, for the longer write pulses, the write

asymmetry changed sign and it was easier to write "1" than "0" with 20 ns pulses. These write asymmetries at nanosecond write times are yet to be fully understood and need to be eliminated. In spite of this WER variability, it is promising that the same MTJ material and patterning process were capable of delivering functioning devices in a broad range of device sizes from 40 nm to 11 nm.
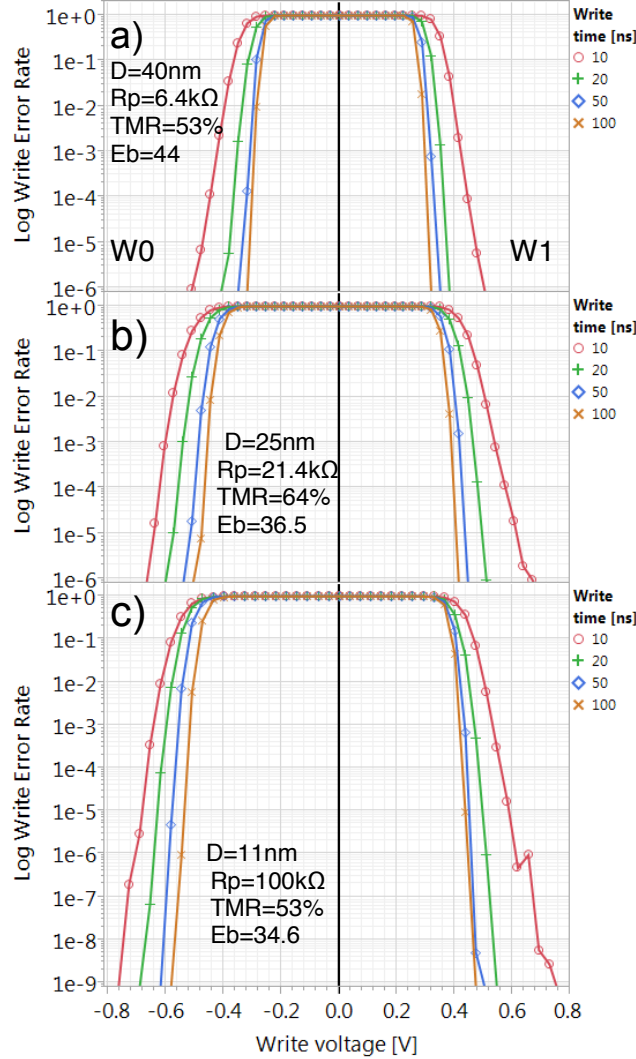

Figure 2 Dependence of write error rates on write voltage at four write times and for three selected device sizes.

The 11 nm device, shown in Fig. 2c, had Rp ~ 100 kΩ. We needed about 0.5 V to reach a 50% switching probability, corresponding to only ~ 5 μA. We needed 0.75 V to reach WER = $7*10^{-10}$, corresponding to only ~ 7.5 μA. This is the first time that ultra-low WER was achieved with such a low write current. To reach WER = 10^{-6}, an average write charge of 6.5 pC and an average energy per switch of ~ 65 fJ were used. These numbers are encouraging, especially since for this device Eb ~ 35 kT, which is close to Eb = 40 kT needed for 10 year retention at room temperature.

Figure 3a shows the average of the write-zero and write-one voltages needed to reach the 10^{-6} WER floor for 655 devices of various sizes. There was a sizable spread of write voltages.

For write voltages higher than 0.7 V we were too close to the breakdown voltage, especially for the smaller devices, so safety margin was too small to complete the testing at higher voltages and shorter write times. All of the data points for absolute write voltages above 0.7 V are extrapolations of the WER data from the 0 - 0.7 voltage range, while the data points below 0.7 V are the experimentally recorded values. With 100 ns write pulses, the write voltages needed to reach WER = 10^{-6} were below 0.5 V.

The solid lines in Fig. 3a are guides to the eye to illustrate how the average write voltage depends on the device diameter. In the single domain model, the write voltage is expected to be independent of the diameter for constant RA [Sun 2000]. Several factors may cause the elevated write voltage at 10 ns. First, junctions edge may be damaged during etching, increasing the RA of the smaller devices and causing write voltage to increase. Second, as in the case of in-plane STT MRAM [Min 2010], ballooning WER(V) shapes were found for about 10% of the devices. These were due to dynamic magnetic defects which were typically detectable at WER< 10^{-3}. Finally, the elevated write voltages in some devices could be test artifacts related to readout noise and the poor stability of one of the states due to unintended Eb asymmetry.
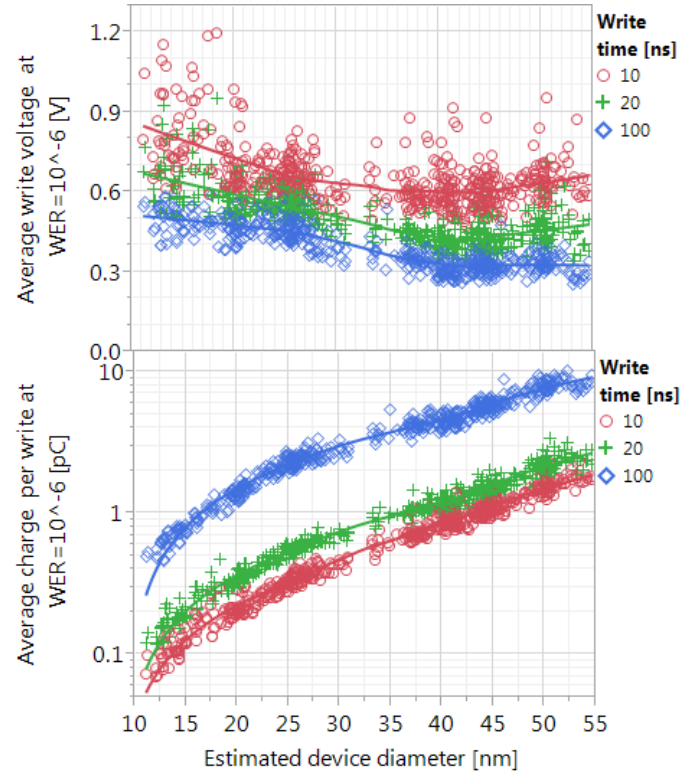

Figure 3 The average write voltage and the average charge per write needed to reach a 10^{-6} WER floor for 655 devices covering the size range from 55 nm to 11 nm.

Figure 3b shows the dependence of the average charge needed to reach the 10^{-6} WER level calculated from the

simplified formula $V*t/Rp$, where V is the write voltage at WER = 10^{-6}, t is the write pulse width, and Rp is the parallel state resistance. For 10 ns writes and to reach the 10^{-6} error floor, we needed average current density for both writes of 8 MA/cm^2. For comparison, the STT quasistatic current density Jc0 is 4 MA/cm^2, so we needed ~2x larger drive to reach 10^{-6} WER floor. The solid lines in Fig. 3b are guides to the eye to illustrate how the average charge per write depends on the device diameter. At approximately 12 nm, several devices required less than 100 fC to reach 10^{-6} WER at 10ns write time, corresponding to ultra-low switching currents below 10 μA. These switching currents are a better match to the maximum current of modern switching transistors, which will enable high density MRAM chips. The expected switching energy, corresponding to 10 ns writes at 10 nm size and 10^{-6} WER, is below 100 fJ, which promises a great improvement in the energy efficiency.

In summary, STT switching is a complicated dynamic phenomenon which needs to be examined in detail on a large and statistically significant sample to ensure the error-free operation of MRAM devices. Proper evaluation of novel STT MRAM materials and stack designs needs to include testing the WER down to an error floor of at least 10^{-6}. It is only the switching parameters at relatively deep WER levels and nanosecond write times that are relevant for the design of future MRAM chips. In this paper we demonstrated that a specific magnetic tunnel junction stack with perpendicular magnetic anisotropy is capable of delivering good STT performance down to 10^{-6} WER in a broad range of device size from 50 nm to 11 nm, on a statistically relevant sample of 655 devices. We further demonstrated an individual 11 nm device switching down to WER = $7*10^{-10}$ using only 7.5 uA.

ACKNOWLEDGMENT

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